ABSTRACT

It is possible to cope with a memory write procedure in which every time data is written into a memory every predetermined amount unit, it is confirmed that readout of the data from the memory has been completed, and then the next write of the data into the memory is performed, and loads on a CPU on a memory readout side can be reduced. In a case where the write of the predetermined amount unit of the data from a PC 2 into an FIFO memory 100 is detected, with respect to the PC 2, a signal is generated which notifies that the readout of the data from the FIFO memory 100 has been completed, and in a case where a stored data amount in the FIFO memory 100 reaches a readout start storage amount, an interrupt signal is generated with respect to a CPU 10 of a PC card 1.